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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,012	10/02/2003	Yasunobu Nakase	67161-112	1468

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EXAMINER	
HO, HOAI V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,012	NAKASE, YASUNOBU	
	Examiner	Art Unit	
	Hoai V. Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/02/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) was considered.

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

2. Claims 1-9 are presented for examination.

Claim Rejections - 35 USC § 112

3. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 4 and 5, a "sense amplifier of a lower hierarchy level ... a sense amplifier of a higher hierarchy level" is unclear and confusing. How do these sense amplifiers relate to a "sense amplifier group" in line 2 of claim 1?

Claim 2, lines 8 and 9 and claim 3, line 7, "complementary signal lines of a lower hierarchy level" is unclear and confusing. How does it relate to a "complementary signal line group" in line 4 of claim 1?

Claims 5, 6 and 8, line 2 and claim 9, line 3, a "predetermined sense amplifier" is unclear and confusing. How does it relate to a "sense amplifier of a lower hierarchy level ... a sense amplifier of a higher hierarchy level" in lines 4 and 5 of claim 1?

Claim 7,

- lines 2-17, "predetermined complementary signal lines" is unclear and confusing. How does it relate to a "complementary signal line group" in line 4 of claim 1?
- line 4, a "sense amplifier of a lower hierarchy level" is unclear and confusing. How does it relate to a "sense amplifier of a lower hierarchy level " in lines 4 and 5 of claim 1?

Similarly, claim 9,

- line 2, "predetermined complementary signal lines" is unclear and confusing. How does it relate to a "complementary signal line group" in line 4 of claim 1?
- line 5, a "sense amplifier of a higher hierarchy level" is unclear and confusing. How does it relate to a "sense amplifier of a higher hierarchy level " in line 5 of claim 1?
- line 5, "than" is unclear and confusing and meaningless in its lines 5-7.

Claims 4, 6 and 8 are rejected due to the rejections of the parent claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada U. S. Patent (USP) No. 5724292.

As per claim 1, Figures 1 and 3 of Wada are directed to a semiconductor memory device comprising: a sense amplifier group (100a and 7) configured in hierarchy to read out data from a memory cell; a complementary signal line group (32) connecting a sense amplifier (100a) of a lower hierarchy level with a sense amplifier (7) of a higher hierarchy level; and a control circuit (110) suppressing a drive of complementary signal lines by the sense amplifier of a lower hierarchy level connected to said complementary signal lines, and rendering active the sense amplifier of a higher hierarchy level connected to said complementary signal lines, before

a potential difference between said complementary signal lines reaches a level of power supply voltage. See column 15, line 16 to column 16, line 19.

As per claims 2-4, Figure 3 of Wada discloses further comprising a write driver group (120 and 7 of fig. 1) configured in hierarchy to write data into a memory cell, wherein a write driver (120) of a lower hierarchy level and a write driver (7 of fig. 1) of a higher hierarchy level are connected by said complementary signal lines and a write designation signal line (33 of fig. 1) , said write driver of a higher hierarchy level outputs write data and inverted data thereof to complementary signal lines of a lower hierarchy level connected to said write driver of a higher hierarchy level, and drives the write designation signal line of a lower hierarchy level connected to said write driver of a higher hierarchy level at a predetermined logic value, and said write driver of a lower hierarchy level is rendered active when the write designation signal line of a higher hierarchy level connected to said write driver of a lower hierarchy level attains said predetermined logic value. See column 14, lines 17-24,

As per claim 5, Figure 3 of Wada discloses wherein a predetermined sense amplifier in said sense amplifier group includes a transmission gate (114) provided between complementary signal lines of a higher hierarchy level and complementary signal lines of a lower hierarchy level, said transmission gate being rendered conductive when in a data write mode.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada U. S. Patent No. 5724292 in view of Yoon et al. U. S. Pub. No. 2004/0022109.

As per claim 6, Wada discloses the predetermined sense amplifier in said sense amplifier group except for including a circuit to fetch a potential of complementary signal lines of a higher hierarchy level connected to said predetermined sense amplifier, and an N channel MOS transistor provided between said circuit and complementary signal lines of a lower hierarchy level connected to said predetermined sense amplifier, said N channel MOS transistor being rendered conductive when in a data write mode.

However, Figure 9 of Yoon discloses a including a circuit (924 and 926) to fetch a potential of complementary signal lines (902 and 960) of a higher hierarchy level connected to said predetermined sense amplifier, and an N channel MOS transistor (948) provided between said circuit and complementary signal lines (DB and DBb) of a lower hierarchy level connected to said predetermined sense amplifier, said N channel MOS transistor being rendered conductive when in a data write mode. It would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Wada' predetermined sense amplifier which utilizes the circuit and the N channel MOS transistor for as taught by Yoon in order to allow for a decrease in chip size ([0058]).

As per claims 7-9, Wada discloses the sense amplifier of a lower hierarchy level except wherein a sense amplifier of a lower hierarchy level connected to said predetermined complementary signal lines, includes an amplify circuit amplifying potentials of said predetermined complementary signal lines, and a P channel MOS transistor provided between

said amplify circuit and said predetermined complementary signal lines, wherein, in a data write mode, said P channel MOS transistor is rendered conductive to have potentials of said predetermined complementary signal lines applied to said amplify circuit, and after said application, said P channel MOS transistor is rendered conductive, and said amplify circuit amplifies said applied potentials at a logic amplitude of power supply voltage, and complementary signal lines of a lower hierarchy level connected to said sense amplifier of a lower hierarchy level connected to said predetermined complementary signal lines are driven based on said amplified potentials.

However, Figure 9 of Yoon discloses wherein the sense amplifier of a lower hierarchy level connected to said predetermined complementary signal lines (902 and 960), includes an amplify circuit (934, 938, 936, 940 and 944) amplifying potentials of said predetermined complementary signal lines, and a P channel MOS transistor (924 and 926) provided between said amplify circuit and said predetermined complementary signal lines. It would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Wada's sense amplifier which utilizes the amplify circuit and the P channel MOS transistor for as taught by Yoon in order to allow for a decrease in chip size ([0058], also see [0070]).

8. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Hirose et al. (USP 5659513), Kozaru (USP 5539691) and Bell (USP 4975877) disclose a semiconductor memory device with write drivers.

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V. Ho whose telephone number is (571) 272-1777. The examiner can normally be reached on 7:00 AM -- 5:30 PM from Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoai V. Ho
Primary Examiner
Art Unit 2818

hvh
October 7, 2004